WHAT IS CLAIMED IS:

1. A semiconductor substrate comprising an insulating underlay and a crystalline silicon layer epitaxially grown thereon, said insulating underlay is a semiconductor substrate comprising a single crystal oxide substrate or a substrate comprising a silicon substrate and a crystalline oxide layer or fluoride layer stacked thereon, wherein a defect density evaluated by a defect density measuring method of measuring a number of pits per unit area formed by immersing in an iodine type etching solution is $7 \times 10^6/cm^2$ or less over an entire depth direction, and surface roughness of said crystalline silicon layer is 0.2 nm or less and 0.05 nm or more.

2. The semiconductor substrate as claimed in Claim 1, wherein said crystalline silicon layer has a X-ray diffraction rocking curve full width at half maximum of a silicon (004) peak parallel to substrate surface is 0.24 degree to 0.03 degree, and X-ray diffraction rocking curve full width at half maximum of a silicon (040) peak perpendicular to substrate surface is 0.18 degree to 0.03 degree.

3. The semiconductor substrate as claimed in Claim 1, wherein said crystalline silicon layer has a X-ray diffraction rocking curve full width at half maximum of

a silicon (040) peak perpendicular to substrate surface is smaller than X-ray diffraction rocking curve full width at half maximum of a silicon (004) peak parallel to substrate surface.

4. The semiconductor substrate as claimed in Claim 1, wherein said crystalline silicon layer has a X-ray diffraction rocking curve full width at half maximum of a silicon (040) peak perpendicular to substrate surface is almost constant over the entire depth direction and 0.18 degree to 0.03 degree.

5. The semiconductor substrate as claimed in Claim 1, wherein, after part of said crystalline silicon layer is thermally oxidized to form a silicon oxide layer on said crystalline silicon layer, an interface level density measured by a charge pumping method is $3 \times 10^{11}/cm^2$ to $1 \times 10^{9}/cm^2$.

6. The semiconductor substrate as claimed in Claim 1, wherein thickness of said crystalline silicon layer is 0.03 μm to 0.7μm.

7. The semiconductor substrate as claimed in Claim 1, wherein said insulating underlay is said single crystal oxide substrate, and said single crystal oxide substrate is a sapphire substrate.

8. The semiconductor substrate as claimed in above Claim 1, wherein said insulating underlay is said laminated substrate, said crystalline oxide layer stacked on silicon substrate as said substrate comprises one of α-Al_2O_3, γ-Al_2O_3, θ-Al_2O_3, $MgO \cdot Al_2O_3$, CeO_2, $SrTiO_3$, $(Zr_{1-x},Y_x)O_y$, $Pb(Zr,Ti)O_3$, $LiTaO_3$, and $LiNbO_3$, and said fluoride layer comprises CaF_2.

9. A method of producing a semiconductor substrate with a low defect density silicon layer formed on an insulating underlay, said method comprising:

(a) a step of forming a first silicon layer on said insulating underlay;

(b) a step of performing a first ion implantation to said first silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by a first heat treatment;

(c) a step of epitaxially growing a silicon layer on said first silicon layer to form a second silicon layer; and

(d) a step of performing a second ion implantation to said second silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by a second heat treatment.

10. A method of producing a semiconductor substrate with

a low defect density silicon layer formed on an insulating underlay, said method comprising:

(a) a step of forming a first silicon layer on said insulating underlay;

(b) a step of performing a first ion implantation to said first silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by a first heat treatment;

(c) a step of heat treating said recrystallized first silicon layer in an oxidizing atmosphere to oxidize part of surface side;

(d) a step of removing silicon oxide film formed in said step (c) by etching;

(e) a step of epitaxially growing a silicon layer on remaining first silicon layer to form a second silicon layer; and

(f) a step of performing a second ion implantation to said second silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by a second heat treatment.

11. The method of producing a semiconductor substrate as claimed in Claim 10, wherein when said remaining first silicon layer is formed to a predetermined thickness, said steps (c) to (d) are repeated two times or more.

12. The method of producing a semiconductor substrate as

claimed in Claim 10 or 11, wherein the silicon layer formed in said step (f) is regarded as said recrystallized first silicon layer formed in said step (b), and said steps (c) to (f) are repeated two times or more.

13. A method of producing a semiconductor substrate with a low defect density silicon layer formed on an insulating underlay, said method comprising:

(a) a step of forming a first silicon layer on said insulating underlay;

(b) a step of heat treating said first silicon layer in an oxidizing atmosphere to oxidize part of surface side;

(c) a step of removing silicon oxide film formed in said step (b) by etching;

(d) a step of epitaxially growing a silicon layer on remaining first silicon layer to form a second silicon layer; and

(e) a step of ion implanting to said second silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by heat treatment.

14. The method of producing a semiconductor substrate as claimed in Claim 13, wherein when said remaining first silicon layer is formed to a predetermined thickness, said steps (b) to (c) are repeated two times or more.

15. The method of producing a semiconductor substrate as

claimed in Claim 13, wherein said silicon layer formed in said step (e) is regarded as said first silicon layer formed in said step (a), and said steps (b) to (e) are repeated two times or more.

SUB a2

16. The method of producing a semiconductor substrate as claimed in any one of Claims 10 to 15, wherein said oxidizing atmosphere contains a mixed gas of oxygen and hydrogen or water vapor.

17. The method of producing a semiconductor substrate as claimed in any one of Claims 10 to 16, wherein temperature of heat treatment in said oxidizing atmosphere is 600°C to 1300°C.

18. The method of producing a semiconductor substrate as claimed in any one of Claims 10 to 16, wherein heat treatment in said oxidizing atmosphere comprises a two-stage heat treatment at different temperatures, wherein initially a high temperature heat treatment is performed at a high temperature and a low temperature heat treatment is performed at a lower temperature subsequent to said high temperature heat treatment.

sub B3

19. The method of producing a semiconductor substrate as claimed in Claim 18, wherein the temperature of the high temperature heat treatment in said oxidizing atmosphere

is 800°C to 1200°C and the temperature of the low temperature heat treatment in said oxidizing atmosphere is 700°C to 1100°C.

Sub a3

20. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 15, wherein a temperature at which a silicon layer is epitaxially grown on said first silicon layer to form a second silicon layer is 550°C to 1050°C.

21. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 15, wherein before said step of epitaxially growing a silicon layer on said first silicon layer to form a second silicon layer, said first silicon layer is heat treated in a hydrogen atmosphere or in a vacuum.

22. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 15, wherein a growing chamber of an apparatus used when a silicon layer is epitaxially grown on said first silicon layer to form a second silicon layer has a base pressure of 10^{-7} Torr or less.

23. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 15, wherein method of epitaxially growing a silicon layer on said first silicon layer

SUB a_3 Concl.

layer to form a second silicon layer is a UHV-CVD method or a MBE method.

24. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 15, wherein when epitaxially growing a silicon layer on said first silicon layer to form a second silicon layer, a growing temperature is set high only in an initial stage of growth.

Sub B3

25. The method of producing a semiconductor substrate as claimed in Claim 24, wherein method of epitaxially growing a silicon layer on said first silicon layer to form a second silicon layer is an APCVD method or a LPCVD method.

SUB a_4

26. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 15, wherein after said step of ion implanting to said second silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by heat treatment, or after said step of epitaxially growing a silicon layer to form a second silicon layer, further comprising a step of heat treatment in hydrogen.

sub B3

27. The method of producing a semiconductor substrate as claimed in Claim 26, wherein temperature of said heat treatment in hydrogen is 800°C to 1200°C.

SUB A5

28. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 15, wherein after said step of ion implanting to said second silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by heat treatment, a surface of the silicon layer is flattened.

sub B3

29. The method of producing a semiconductor substrate as claimed in Claim 28, wherein said method of flattening surface of said silicon layer is a chemical and/or mechanical polishing.

SUB A6

30. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 29, wherein said step of forming a first silicon layer on said insulating underlay is a step of epitaxially growing said first silicon layer on said insulating underlay.

31. The method of producing a semiconductor substrate as claimed in any one of Claims 9 to 30, wherein said insulating underlay is a single crystal oxide substrate.

sub B3

32. The method of producing a semiconductor substrate as claimed in Claim 31, wherein said insulating underlay is a sapphire substrate.

SUB A7

33. The method of producing a semiconductor substrate as

SUB a7 cont

claimed in any one of Claims 9 to 30, wherein said insulating underlay is a laminated substrate comprising crystalline oxide layer or fluoride layer stacked on a silicon substrate as a substrate.

Sub B3

34. The method of producing a semiconductor substrate as claimed in Claim 33, wherein said crystalline oxide layer comprises one of α-Al_2O_3, γ-Al_2O_3, θ-Al_2O_3, $MgO{\cdot}Al_2O_3$, CeO_2, $SrTiO_3$, $(Zr_{1-x},Y_x)O_y$, $Pb(Zr, Ti)O_3$, $LiTaO_3$, and $LiNbO_3$, and said crystalline fluoride layer comprises CaF_2.

SUB a8

35. A semiconductor substrate produced by the method as claimed in any one of Claims 9 to 34.

36. The semiconductor substrate as claimed in any one of Claims 1 to 8, characterized in that it is produced by the method as claimed in any one of Claims 9 to 34.

37. A semiconductor device having a semiconductor substrate, wherein said semiconductor substrate is a semiconductor substrate as claimed in any one of Claims 1 to 8 is used, whereby improving device characteristics.

38. The semiconductor device as claimed in Claim 37, wherein said semiconductor device is MOSFET, and said device characteristic improved by using the semiconductor substrate as claimed in any one of Claims 1 to 8 as

SUB a_8 Cont

semiconductor substrate thereof is at least one of trans-conductance, cut-off frequency, flicker noise, electrostatic discharge, drain breakdown voltage, dielectric breakdown charge amount, and leakage current characteristics.

39. The semiconductor device as claimed in Claim 38, wherein said MOSFET uses the semiconductor substrate as claimed in any one of Claims 1 to 8 as the semiconductor substrate thereof, is a MOSFET formed on a semiconductor substrate with a thickness of crystalline silicon layer of 0.03 μm to 0.7 μm, and no kink appears in a current - voltage measurement, a drain breakdown voltage as measured using a gate length of 0.8 μm is 7V or more, and an input gate voltage spectral density representing flicker noise is 3×10^{-12} V^2/Hz or less at a measuring frequency of 100 Hz.

40. The semiconductor device as claimed in Claim 37, wherein said semiconductor device is a bipolar transistor, and device characteristic improved by using the semiconductor substrate as claimed in any one of Claims 1 to 8 as the semiconductor substrate thereof is at least one of trans-conductance, cut-off frequency, collector current, leakage current, and current gain.

41. The semiconductor device as claimed in Claim 37,

SUB a8 Cont

wherein said semiconductor device is a diode, and device characteristic improved by using the semiconductor substrate as claimed in any one of Claims 1 to 8 as semiconductor substrate thereof is at least one of reverse bias leakage current, forward bias current, and diode factor.

42. The semiconductor device as claimed in Claim 41, wherein said diode is a pin photodiode formed on the semiconductor substrate as claimed in any one of Claims 1 to 8 as the semiconductor substrate thereof having a thickness of crystalline silicon layer of 0.03 to 0.7 μm, having a pin area width of each 1 μm, and a dark current measured under a condition applied with a 2V reverse bias is 10^{-11} A or less, and a photocurrent under light irradiation of 1W/cm^2 intensity at wavelength 850 nm is 10^{-10} A or more.

43. The semiconductor device as claimed in Claim 37, wherein said semiconductor device is a semiconductor device integrated circuit, and device characteristic improved by using the semiconductor substrate as claimed in any one of Claims 1 to 8 as semiconductor substrate thereof is at least one of frequency characteristic, noise characteristic, amplification characteristic, and power consumption characteristic.

44. A semiconductor device having a semiconductor substrate, wherein the semiconductor substrate is produced by the method as claimed in any one of Claims 9 to 34 is used, whereby improving device characteristics.

45. The semiconductor device as claimed in Claim 44, wherein said semiconductor device is a MOSFET, and said device characteristic is at least one of trans-conductance, cut-off frequency, flicker noise, electrostatic discharge, drain breakdown voltage, dielectric breakdown charge amount, and leakage current characteristics.

46. The semiconductor device as claimed in Claim 45, wherein said MOSFET is formed on the semiconductor substrate with a thickness of crystalline silicon layer of 0.03 μm to 0.7 μm, and no kink appears in a current - voltage measurement, a drain breakdown voltage as a measured using a gate length of 0.8 μm is 7V or more, and an input gate voltage spectral density representing flicker noise is 3×10^{-12} V^2/Hz or less at a measuring frequency of 100 Hz.

47. The semiconductor device as claimed in Claim 44, wherein said semiconductor device is a bipolar transistor, and said device characteristic is at least one of trans-conductance, cut-off frequency, collector current,

leakage current, and current gain.

48. The semiconductor device as claimed in Claim 44, wherein said semiconductor device is a diode, and said device characteristic is at least one of reverse bias leakage current, forward bias current, and diode factor.

SUB a9

49. The semiconductor device as claimed in Claim 48, wherein said diode is a pin photodiode formed on the semiconductor substrate as claimed in any one of Claims 1 to 8, wherein said semiconductor substrate has a thickness of crystalline silicon layer of 0.03μm to 0.7 μm, and a pin area width of each 1μm, and a dark current measured with a 2V reverse bias is 10^{-11} A or less, and photocurrent under light irradiation of $1 W/cm^2$ intensity at wavelength 850 nm is 10^{-10} A or more.

50. The semiconductor device as claimed in Claim 44, wherein said semiconductor device is a semiconductor integrated circuit, and said device characteristic is at least one of frequency characteristic, noise characteristic, amplification characteristic, and power consumption characteristic.

51. A method of producing a semiconductor device comprising an insulating underlay and a silicon layer formed thereon, said method comprising:

(a) a step of forming a first silicon layer on said insulating underlay;

(b) a step of performing a first ion implantation to said first silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by a first heat treatment;

(c) a step of epitaxially growing a silicon layer on said first silicon layer to form a second silicon layer;

(d) a step of performing a second ion implantation to said second silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by a second heat treatment; and

(e) after heat treating said silicon layer formed in said step (d) in an oxidizing atmosphere to oxidize part of surface side, a step of removing said formed silicon oxide film by etching to adjust said silicon layer to a desired thickness.

52. A method of producing a semiconductor device comprising an insulating underlay and a silicon layer formed thereon, said method comprising:

(a) a step of forming a first silicon layer on said insulating underlay;

(b) a step of performing a first ion implantation to said first silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by a first heat treatment;

(c) a step of heat treating said recrystallized first silicon layer in an oxidizing atmosphere to oxidize part of surface side;

(d) a step of removing said silicon oxide film formed in said step (c) by etching;

(e) a step of epitaxially growing a silicon layer on remaining first silicon layer to form a second silicon layer;

(f) a step of performing a second ion implantation to said second silicon layer to make a deep part of an interface amorphous, and recrystallzing said amorphous layer by a second heat treatment;

(g) after heat treating said silicon layer formed in said step (f) in an oxidizing atmosphere to oxidize part of surface side, a step of removing said formed silicon oxide film by etching to adjust said silicon layer to a desired thickness.

53. The method of producing a semiconductor device as claimed in Claim 52, wherein when forming said remaining first silicon layer to a predetermined thickness, said steps (c) to (d) are repeated two times or more.

54. The method of producing a semiconductor device as claimed in any one of Claims 52 to 53, wherein said silicon layer formed in said step (f) is regarded as said recrystallized first silicon layer formed in said step (b),

and said steps (c) to (f) are repeated two times or more.

55. A method of producing a semiconductor device comprising an insulating underlay and a silicon layer formed thereon, said method comprising:

(a) a step of forming a first silicon layer on said insulating underlay;

(b) a step of heat treating said first silicon layer in an oxidizing atmosphere to oxidize part of surface side;

(c) a step of removing said silicon oxide film formed in said step (b) by etching;

(d) a step of epitaxially growing a silicon layer on said remaining first silicon layer to form a second silicon layer;

(e) a step of ion implanting to said second silicon layer to make a deep part of an interface amorphous, and recrystallizing said amorphous layer by heat treatment; and

(f) after heat treating said silicon layer formed in said step (e) in an oxidizing atmosphere to oxidize part of surface side, a step of removing said formed silicon oxide film by etching to adjust said silicon layer to a desired thickness.

56. The method of producing a semiconductor device as claimed in Claim 55, wherein when forming said remaining first silicon layer to a predetermined thickness, said

steps (b) to (c) are repeated two times or more.

57. The method of producing a semiconductor device as claimed in any one of Claims 55 to 56, wherein said silicon layer formed in said step (e) is regarded as said first silicon layer formed in said step (a), and said steps (b) to (e) are repeated two times or more.

SUB Q10

58. The method of producing a semiconductor device as claimed in any one of Claims 51 to 57, wherein after said step of ion implanting to said second silicon layer to make a deep part of an interface amorphous and recrystallizing said amorphous layer by heat treatment, or after said step of epitaxially growing said silicon layer to form a second silicon layer, further comprising a step of heat treatment in hydrogen.

59. The method of producing a semiconductor device as claimed in any one of Claims 51 to 57, wherein after said step of ion implanting to said second silicon layer to make a deep part of an interface amorphous and recrystallizing said amorphous layer by heat treatment, a surface of said silicon layer is flattened by chemical and/or mechanical polishing.